WHAT IS CLAIMED IS:

1. A digitizer for converting an analog signal output from an electronic device to a digital signal, comprising:

an A/D converter operable to sequentially convert the analog signal output from said electronic device to a digital signal at predetermined time intervals; and

a digital filter operable to output a corrected signal obtained by multiplying said digital signal converted by said A/D converter by a correction coefficient based on a phase error between an ideal sampling timing at which said A/D converter is to sample said analog signal and an actual timing at which said A/D converter sampled said analog signal.

2. A digitizer as claimed in claim 1, wherein said digital filter has an impulse response function given thereto for calculating said correction coefficient, and

said digital filter outputs said corrected signal obtained by calculating convolution of said correction coefficient, that is a value of said impulse response function corresponding to a timing away from said ideal sampling timing by said phase error, and values of said digital signal.

3. A digitizer for converting an analog signal output from an electronic device to a digital signal, comprising:

N A/D converters operable to convert the analog signal output from said electronic device to digital signals at different sampling timings by turns, N being an integer equal to or larger than 2; and

N digital filters operable to output corrected signals, each of said corrected signals being obtained by multiplying

one of said digital signals output from an associated one of said N A/D converters by a correction coefficient based on a phase error between an ideal sampling timing at which said associated A/D converter is to sample said analog signal and an actual sampling timing at which said associated A/D converter sampled said analog signal.

4. A digitizer as claimed in claim 3, wherein each of said N digital filters includes a memory in which an impulse response function for calculating said correction coefficient is stored, and

said N digital filters output said corrected signals each obtained by calculating convolution of said correction coefficient, that is a value of said impulse response function corresponding to a timing away from said ideal sampling timing by said phase error of said associated A/D converter, and values of said digital signal converted by said associated A/D converter.

5. A digitizer as claimed in claim 4, wherein said memory stores said impulse response function based on gain characteristics of said associated A/D converter.

6. A digitizer as claimed in claim 4 or 5, wherein said memory stores said impulse response function based on frequency characteristics of said associated A/D converter.

7. A digitizer as claimed in claim 3, wherein each of said N digital filters include a memory for storing as said correction coefficient a value of an impulse response function of said digital filter at said actual sampling timing of said associated

A/D converter, and

said N digital filters output said corrected signals each obtained by calculation of convolution of values of said digital signal converted by said associated A/D converter and said correction coefficient.

8. A digitizer as claimed in claim 7, wherein said memory stores said correction coefficient based on gain characteristics of said associated A/D converter.

9. A digitizer as claimed in claim 7 or 8, wherein said memory stores said correction coefficient based on frequency characteristics of said associated A/D converter.

10. A digitizer as claimed in claim 3, further comprising an interleaving unit operable to generate a data sequence obtained by arranging said corrected signals respectively output from said N digital filters in a predetermined order.

11. A digitizer as claimed in claim 3, further comprising a decimation data generation unit operable to calculate a sum of said corrected signals respectively output from said plurality of digital filers to generate decimation data, wherein

each of said N digital filters multiplies said digital signal output from said associated A/D converter by said correction coefficient based on:

a phase error between said ideal sampling timing at which said associated A/D converter is to sample said analog signal and said actual sampling timing at which said associated A/D converter sampled said analog signal; and

a phase difference between said ideal sampling timing of said associated A/D converter and an ideal sampling timing of one of said N A/D converters that is used as a reference A/D converter.

12. A digitizer as claimed in claim 11, wherein each of said N digital filters includes a memory for storing a plurality of correction coefficients obtained by decomposing a predetermined impulse response function by a polyphase decomposition and multiplying results of the polyphase decomposition by a coefficient based on said phase error, and

said N digital filters output said corrected signals obtained by calculation of convolution of said plurality of correction coefficients and said digital signals.

13. A digitizer as claimed in claim 12, wherein said memory of each of said N digital filters stores, as said plurality of correction coefficients, values obtained by multiplying values of said impulse response function at said ideal sampling timings of said associated A/D converter by said coefficient based on said phase error.

14. A digitizer as claimed in claim 13, wherein said memory of each of said N digital filters stores said plurality of correction coefficients based on a function obtained by moving said impulse response function on a time axis by a difference between a phase of said ideal sampling timing of said associated A/D converter and a phase of said ideal sampling timing of said reference A/D converter, and said phase error.

15. A digitizer for converting an analog signal output from

an electronic device to a digital signal, comprising:

N A/D converters operable to convert the analog signal output from said electronic device to digital signals at different sampling timings by turns, N being an integer equal to or larger than 2;

a first interleaving unit operable to generate a first data sequence obtained by arranging said digital signals converted by said N A/D converters in a predetermined order to output said first data sequence;

N digital filters operable to receive said first data sequence output from said first interleaving unit, to calculate convolution of correction coefficients based on phase errors between ideal sampling timings at which said N A/D converters are to sample said analog signal and actual sampling timings at which said N A/D converters sampled said analog signal and said first data sequence so that each of said N digital filters generate and output decimation data containing less number of data units than data units in said first data sequence; and

a second interleaving unit operable to generate a second data sequence obtained by arranging said data units in said decimation data output from each of said N digital filters in a predetermined order.

16. A digitizer as claimed in claim 15, wherein said N digital filters include memories operable to store impulse response functions for calculating said correction coefficients, and

said N digital filters output signals obtained by convolution of values of said impulse response functions corresponding to timings away from said ideal sampling timings by said phase errors of associated A/D converters and values of said digital signals converted by said associated A/D

converters, respectively.

17. A testing apparatus for testing an electronic device, comprising:

a pattern generator operable to generate a pattern signal and an expected-value signal;

a waveform shaping unit operable to shape a waveform of said pattern signal generated by said pattern generator;

a device contact unit, onto which said electronic device is to be placed, operable to supply said pattern signal shaped by said waveform shaping unit to said electronic device and to receive an analog signal output from said electronic device;

a digitizer operable to convert said analog signal output from said electronic device to a digital signal; and

a determination unit operable to determine based on said expected-value signal output from said pattern generator and a signal output from said digitizer whether or not said electronic device is defective, wherein

said digitizer includes an A/D converter operable to sequentially convert said analog signal output from said electronic device to digital signals at predetermined intervals, and outputs corrected signals obtained by multiplying said digital signals by a correction coefficient based on a phase error between ideal sampling timings at which said A/D converter is to sample said analog signal and sampling timings at which said A/D converter sampled said analog signal.

18. A testing apparatus for testing an electronic device, comprising:

a pattern generator operable to generate a pattern signal and an expected-value signal;

a waveform shaping unit operable to shape a waveform of said pattern signal generated by said pattern generator;

a device contact unit, onto which said electronic device is to be placed, operable to supply said pattern signal shaped by said waveform shaping unit to said electronic device and to receive an analog signal output from said electronic device;

a digitizer operable to convert said analog signal output from said electronic device to a digital signal; and

a determination unit operable to determine based on said expected-value signal output from said pattern generator and a signal output from said digitizer whether or not said electronic device is defective, wherein said digitizer includes:

N A/D converters operable to convert said analog signal output from said electronic device to digital signals at different sampling timings, N being an integer equal to or larger than 2; and

N digital filters operable to output corrected signals obtained by multiplying said digital signals output from said N A/D converters by correction coefficients, and

said N digital filters multiply said digital signals converted by associated A/D converters by said correction coefficients based on phase errors between ideal sampling timings at which said associated A/D converters are to sample said analog signal and sampling timings at which said N A/D converters sampled said analog signal.

19. A testing apparatus as claimed in claim 18, wherein said digitizer further includes a decimation data generation unit operable to calculate a sum of said corrected signals respectively output from said plurality of digital filters to generate decimation data, wherein

said N digital filters output said corrected signals obtained by multiplying said digital signals converted by said associated A/D converters by said correction coefficients based on:

phase errors between said ideal sampling timings at which said associated A/D converters are to sample said analog signal and said actual sampling timing at which said N A/D converters sampled said analog signal; and

phase differences between said ideal sampling timings of said associated A/D converters and ideal sampling timings of one of said N A/D converters that is used as a reference.

20. A testing apparatus for testing an electronic device, comprising:

a pattern generator operable to generate a pattern signal and an expected-value signal;

a waveform shaping unit operable to shape a waveform of said pattern signal generated by said pattern generator;

a device contact unit, onto which said electronic device is to be placed, operable to supply said pattern signal shaped by said waveform shaping unit to said electronic device and to receive an analog signal output from said electronic device;

a digitizer operable to convert said analog signal output from said electronic device to a digital signal; and

a determination unit operable to determine based on said expected-value signal output from said pattern generator and a signal output from said digitizer whether or not said electronic device is defective, wherein said digitizer includes:

N A/D converters operable to convert said analog signal output from said electronic device to digital signals at different sampling timings by turns, N being an integer equal

to or larger than 2;

a first interleaving unit operable to generate and output a first data sequence obtained by arranging said digital signals converted by said N A/D converters in a predetermined order;

N digital filters operable to receive said first data sequence output from said first interleaving unit and to calculate convolution of correction coefficients, based on phase errors between ideal sampling timings at which said N A/D converters are to sample said analog signal and actual sampling timings at which said N A/D converters sampled said analog signal, and said first data sequence to generate and output decimation data, said decimation data of each of said N digital filters containing less number of data units than data units in said first data sequence; and

a second interleaving unit operable to generate a second data sequence obtained by arranging said data units in said decimation data output from said N digital filters in a predetermined order.